Remarks

Claims 1-20 remain in this application. Claims 1 and 9 have been amended. Claims 1, 9 and 15 are independent claims.

A. Patentability of Claim 1

Claim 1 was rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Takinosawa. Applicant has amended claim 1 to further distinguish the invention from the cited prior art. Claim 1 has been amended to describe the tester portion of the integrated circuit as a plurality of functionally identical testers, with the testers being connected to individually test each said SERDES, and each of the testers being enabled to detect performance characteristics of individual SERDESs independently of the other testers.

The Office action cited Takinosawa as teaching that a plurality of testers is integrated with a SERDES. Specifically, the USB physical layer 18 comprises a built-in self-test (TX-BIST) circuit 35, a multiplexer 36, and a built-in self-analyzer circuit 49. The Office action identified these three components of the USB physical layer as being a "plurality of testers." The TX-BIST circuit 35 may operate in the normal mode (paragraph [0025]) or in the BIST mode. The mode of operation is selectable and controlled by the TX-BIST enable signal which may be generated by the link layer 16 or by physical layer 18 (Takinosawa: paragraph [0028]). When enabled in BIST mode, the TX-BIST circuit generates pseudo random data words for use by the multiplexer 36.

The multiplexer 36 of Takinosawa is a second of the plurality of testers as referenced by the Office action. The multiplexer merely selects one of two data buses. In normal mode, with TX-BIST enable inactive, the data from data bus 21 is accepted and passed onto register 37 of transmitter section 31. In BIST mode, with TX-BIST enable active, the data from the built-in test circuit (35) is accepted and passed onto the transmitter section.

The BIST analyzer circuit 49, the third of the plurality of testers as referenced by the Office action (Takinosawa: paragraph [0031]), when in BIST mode and when enabled by the RX-BIST enable signal being active, receives decoded unstuffed data via bus 25 from register 48 of receiver section 32. An error signal is generated if the expected data is not received.

None of the Takinosawa "testers" (i.e., the self-test (TX-BIST) circuit 35, multiplexer 36 or built-in self-test analyzer circuit 49) cited by the Office action functions individually as described for each tester of the claimed invention. In accordance with the amended claim, each tester of the claimed invention is functionally identical to the other testers and is enabled to detect performance characteristics independently of the testers. On the other hand, the Takinosawa components that are cited as being "testers" are functionally dissimilar. Equally importantly, the Takinosawa components that are cited as being "testers" are dependently enabled. For example, the "tester 35" (i.e., the TX-BIST circuit 35 of Takinosawa) is dependently enabled since testing capability is dependent upon exchanges of data with the "tester 36" (i.e., the multiplexer 36). Therefore, Applicant respectfully asserts that the amendments to claim 1 place the claim and its dependent claims in a condition for allowance.

The Office action further cited Takinosawa as disclosing that it is possible to conduct self-tests on two chips (USB physical layers) or a plurality of SERDESs and testers. Applicant respectfully points out that the tester as disclosed in Takinosawa [0048] is limited to only testing two chips or USB physical layers. As disclosed, the first chip is controlled to act as a transmitter and a second chip is controlled to act as a receiver. Moreover, for the disclosed test to be successful, a cable is used to interconnect the first and second chips. This clearly indicates that the two USB layers (or SERDESs) are completely separate and not integrated or embedded within the same integrated circuit. The claimed invention describes an integrated circuit comprising a plurality of SERDESs. The claimed integrated circuit having a plurality of SERDESs is not anticipated by the Takinosawa teaching of a plurality of integrated circuits, with each having a single "SERDES."

Therefore, Applicant respectfully asserts there is a material difference between the amended claim 1 and the cited prior art and requests reconsideration of the patentability of amended claim 1 and its dependent claims.

B. Patentability of Claim 9

Claim 9 was rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Takinosawa. Applicant has amended claim 9 to further distinguish the invention from the cited prior art. Specifically, the claimed integrated circuit includes a single substrate on which the integrated circuitry

is fabricated. By amending the claim, it is made clear that the core circuitry, SERDESs, functional test interfaces (FTIs), functional test controllers (FTCs) and input/output controller (IOC) are components of the same integrated circuit fabricated onto the same semiconductor substrate.

Takinosawa (Fig. 1) teaches that a USB Interface 17 is formed by the USB link layer 16 and the USB physical layer 18. Takinosawa, in paragraph [0048], teaches that a self test may be performed on two chips (e.g., two USB physical layers). The first chip is activated to function as a transmitter and the second chip is activated to function as a receiver. This test requires the use of a cable to interconnect the first and second chips. Only the requisite trigger signals are required to make the USB physical layer operational. The requisite trigger signal would emanate from the USB link layer or core circuitry and would be delivered to the appropriate USB physical layer chip. Takinosawa does not teach that the USB physical layer chips and the USB link layer are components of the same integrated circuit fabricated onto the same semiconductor substrate. Therefore, Takinosawa does not anticipate claim 9, as amended.

In addition, since each combination of a USB physical layer 18 (or SERDES) and tester exists on a separate chip from another SERDES and tester combination, Takinosawa does not teach that a plurality of SERDESs/testers may be integrated onto the same semiconductor substrate. The Office action alleged that the TX-BIST circuit 35 and the multiplexer 36 of Takinosawa anticipate the FTI and FTC, respectively, of Applicant's claimed invention. The TX-BIST circuit and multiplexer are components of the SERDES and "tester" (or USB physical layer). Because there is no teaching in Takinosawa regarding integrating a plurality of SERDESs and testers onto the same semiconductor substrate, it follows that there is no teaching that a plurality of FTIs and a plurality of FTCs may be integrated onto the same semiconductor substrate.

In view of the remarks made in support of amended claim 9, Applicant respectfully asserts a material difference exists between the amended claim and the cited prior art. Reconsideration of the patentability of amended claim 9 and its dependent claims is requested.

C. Patentability of Claim 15

Claim 15 was rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Takinosawa. The Office action cited Takinosawa

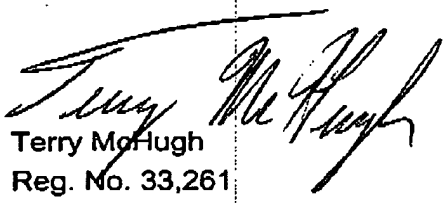
(page 6, paragraph [0048]) as disclosing a plurality of test interfaces and test controllers. The cited reference involves the performance of a self test on two chips (e.g., USB physical layers). As is known to one of ordinary skill in the art, the word "chip" refers to an integrated circuit on a unitary substrate. The Takinosawa statements regarding "two chips" clearly teach that there are two separate integrated circuits. Takinosawa in paragraph [0048] also discloses that the self test requires the use of a cable to interconnect the first and second chips. This is a further indication that the two chips (i.e., integrated circuits) are separate from each other.

The claimed invention is a method of embedding a plurality of test interfaces within the same integrated circuit. Claim 15 also describes embedding test controllers within the same integrated circuit as the test interfaces, such that each test controller is specific to a test interface. The test interfaces and test controllers of the claimed invention are embedded within the same integrated circuit, whereas in the cited prior art, the test interfaces and test controllers exist within separate integrated circuits.

Therefore, Applicant respectfully asserts that a material difference exists between the claimed invention and the cited prior art. Reconsideration of the patentability of claim 15 and its dependent claims is requested.

Applicant respectfully requests reconsideration of the claims in view of the amendments and remarks made herein. A notice of allowance is earnestly solicited. In the case that any issues regarding this application can be resolved expeditiously via a telephone conversation, Applicant invites the Examiner to call Terry McHugh at (650) 969-8458.

Respectfully submitted,



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